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In Situ Synthesis of High Density sub-50 nm ZnO Nanopatterned Arrays Using Diblock Copolymer Templates

Vignesh Suresh,[†] Meiyu Stella Huang,[†] M.P. Srinivasan,[*,†] and Sivashankar Krishnamoorthy[*,‡,§]

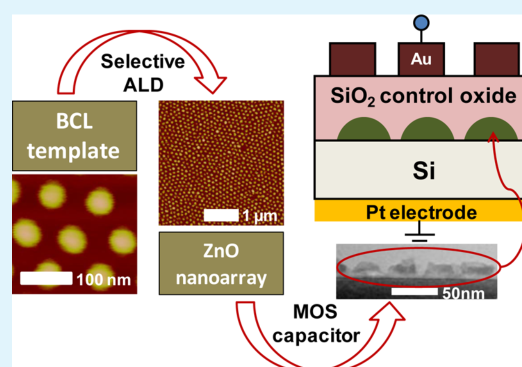
[†]Department of Chemical and Biomolecular Engineering, National University of Singapore, Blk E5, 4 Engineering Drive 4, Singapore 117576

[‡]Patterning and Fabrication group, Institute of Materials Research and Engineering (IMRE), Agency for Science Technology and Research (A*STAR), 3, Research Link, Singapore 117602

[§]Science et Analyse des Materiaux unit (SAM), Centre de Recherche Public-Gabriel Lippmann, 41, rue du Brill, Belvaux, Luxembourg 4422

Supporting Information

ABSTRACT: Fabrication of high density (~155 Gbit in^{-2}) ZnO nanopatterns through in situ decomposition of Zn precursors inside diblock copolymer templates and their application as charge storage centers in nonvolatile memory devices is described. The fabrication is performed in a highly controlled fashion with the resulting ZnO nanopatterned arrays exhibiting diameters of 38 nm and heights of 14 nm offering sub-50 nm feature resolutions. The ZnO nanopatterns are naturally n-type due to the presence of zinc interstitials and oxygen vacancies that act as defect levels in trapping charge carriers. Test capacitors (metal-oxide-semiconductor, MOS) constructed using nanopatterns formed on p-Si exhibited a large flatband voltage shift of about ~2.2 V for a low operating voltage of 10 V. A high charge trap density of 3.47×10^{18} cm^{-3} combined with a good retention capacity is observed with low tunneling oxide (thermally grown) thickness of 3 nm. This demonstrates the significant promise of the ZnO nanopatterned arrays to act as charge storage centers for potential application in nonvolatile flash memory devices. The charge trapping characteristics, the capacitance−voltage measurements, and the potential of ZnO nanopatterns as charge storage centers in fabricating nonvolatile memory devices are discussed.



KEYWORDS: *atomic layer deposition, ZnO, nanopattern, nanoarrays, block copolymer, self-assembly, sub-50 nm patterning, flash memory device, nanolithography, nanoparticle*

1. INTRODUCTION

Nanopatterning of semiconducting metal oxides on silicon is widely considered as a potential combination in advanced silicon electronics such as memory devices, diodes, and solid state lighting. Several top-down and bottom-up techniques are known to produce desired patterns of nanofeatures catering to the needs of the silicon industry. Some of the state-of-the-art techniques that can produce macroscopic nanoarrays are nanoimprint lithography (NIL),[1,2] laser interference lithography,[3] photolithography,[4] nanostencils,[5] block copolymer lithography (BCL),[6,7] nanosphere lithography,[8] and anodized alumina.[9,10] The feasibility of delivering templates at high resolutions, process compatibility and flexibility with existing manufacturing tools, and ability for integration within devices are some of the key factors that influence the preferred choice of techniques.

ZnO is one of the widely investigated materials in the context of their use in LEDs,[11] memory devices,[12] antireflection coatings,[13] self-cleaning surfaces,[14] solar cells,[15] and piezoelectric actuators[16] owing to its intrinsic n-type conductivity,[17] wide band gap of 3.37 eV, and other attractive optoelectronic properties. There are reports on the different fabrication methodologies used to produce patterned arrays of ZnO such as hydrothermal synthesis,[3,18] metal oxide chemical vapor deposition (MOCVD),[19] vapor−liquid−solid (VLS) growth,[1,10,20] template-guided electro deposition of zinc,[21] colloidal template assisted patterning,[22,23] and direct patterning of sol−gel precursors.[2] For specific applications such as flash memory devices, a high degree of compatibility between the nanopatterned material and Si is needed, where residues of catalyst and precursor should not influence the device performance. This calls for an improved, contamination-free and cleaner fabrication technique.

ZnO nanopatterns formed on different substrates offer an interesting opportunity to investigate and study various material properties in combination with the substrate properties. The

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nature of doping in silicon which can be either n-type or p-type has a distinct effect on the electrical and electronic properties of the material that is deposited on top of it. ZnO nanostructures generally have a lot of zinc interstitials and oxygen vacancies making them intrinsically n-type.[24,25] The electrical behavior of the ZnO nanofeatures on p-Si is different from that of n-Si, and this characteristic is exploited in fabricating diodes or schottky barriers,[26] transistors, or capacitors.[25]

There has been an increasing interest toward exploiting the ZnO nanostructures for fabricating electronic devices compatible with silicon technology. There are many reports on the utilization of ZnO nanostructures in memory devices,[27] thin film transistors,[28,29] diodes,[30] etc. Earlier reports on the ZnO nanofilm based memory devices[31−33] built on Si describe the electrical characteristics of the ZnO nanofilm. However, they fall short in meeting performance requirements such as memory window, scalability of tunnel oxide layer, program/erase voltages, and writing speeds.[34,35] This calls for a new device structure targeting these issues. In our earlier work,[36,37] we have shown applications of ZnO nanopatterns for charge trap flash memories with sub-100 nm feature/spatial resolutions by employing a combination of block copolymer (BCP) self-assembly and nanoimprint lithography (NIL). In those approaches, we have employed BCP templates to create high-resolution pillar molds for NIL. The BCP-NIL process was subsequently used to realize nanoporous templates to direct selective growth (by atomic layer deposition or ALD) or deposition (by RF sputtering) of ZnO.[36,37] ZnO nanopatterns on p-Si obtained in these two instances exhibited high hole storage densities of 2.3×10^{18} cm^{-3} [36] and 7.39×10^{18} cm^{-3} [37] programmed at a lower operating voltage of 10 V. Although attractive for creating well-defined ZnO nanopatterns, the BCL-NIL approach is limited in certain ways; viz., the feature width and the spacing of the patterns is determined by the mold, thus requiring different molds to tune pattern dimensions; the approach involves three pattern-transfer steps: the realization of NIL molds, formation of nanoporous templates, and subsequent transfer to ZnO patterns. While the process is still scalable and can be potentially automated, it is desirable to look for simpler solutions with reduced process complexity, yet offering equivalent benefits for nonvolatile memories. In this direction, we report here a novel way of producing high-density ZnO nanopatterns with sub-50 nm feature widths, through in situ synthesis using block copolymer templates. The process uses selective decomposition of volatile and highly reactive zinc precursors within the core of reverse micelles on the surface. The exposure to precursors with precise dosage is performed within an ALD reactor. In an earlier work,[38] we demonstrated the feasibility of the approach for nanopatterning of TiO_2. In situ synthesis of inorganic materials such as TiO_2 and Al_2O_3 through ALD using organometallic precursors within phase-separated copolymer thin films has also been reported in the literature.[39,40] However, the coat-and-use possibility using reverse micelle templates offers significant processing simplicity. The process allows inherent advantages in the use of block copolymers toward engineering resulting patterns at the molecular level (through degree of polymerization, block ratios, and block composition). In addition, the reverse micelle approach has inherent additional controls through solvent quality, deposition speeds, micelle concentrations, and relative humidity. Beyond the template tunability, the ALD process brings in the process control with high degree of precision in exposure to precursors. ZnO patterns demonstrated in this work with sub-50 nm feature resolutions at high feature densities, are found to exhibit high hole storage densities and retentivity, thus serving as a promising means for realizing high performance charge-trap flash memories.

2. EXPERIMENTAL SECTION

2.1. Materials. 2-Propanol and acetone were obtained as anhydrous solvents with purity >99% from Sigma-Aldrich Pte Ltd. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Silicon wafers with thermally grown oxide were obtained from Global Foundries, Singapore. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland).

2.2. Method. The silicon substrates were diced and cleaned by ultrasonicating in acetone followed by 2-propanol and finally exposed to UV/ozone (UV-1, SAMCO Inc., Kyoto, Japan) for 10 min. Ellipsometry (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA) was used to measure thickness of the oxide layers. The block copolymer templates used to guide the patterning of ZnO was obtained by spin coating a 0.5% (w/w) solution of reverse micelles of polystyrene-*block*-poly(vinylpyridine) (PS-*b*-PVP, MW 80.5 kDa, f_{PS} 0.5, PDI 1.1) in *m*-xylene at 3000 rpm (CEE model 100CB spinner, Brewer Science Inc., MO, USA). The coated micelles were then subjected to atomic layer deposition of ZnO performed using an ALD system (TFS200, Beneq, Vantaa, Finland) at 70 °C. Diethyl zinc (used as the Zn precursor) and deionized water were introduced into a viscous flow ALD chamber in pulses as $(C_2H_5)_2Zn$ (17 mTorr, 0.3 s)/N_2 purge (2 mTorr, 2 s)/H_2O (17 mTorr, 0.3 s)/N_2 purge (2 mTorr, 2 s) (refer to Figure S1 of the Supporting Information for a representative pressure vs time plot for an ALD cycle). N_2 was used both as a carrier and as purge gas. Oxygen plasma exposure for removing the polymer was performed using a reactive ion etcher (Oxford plasmlab100, Oxford Instruments, UK) at 65 mTorr, 30 W, and 20 sccm O_2 for 15 min. Atomic force microscopy (AFM, Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA), field emission scanning electron microscopy (FESEM, JEOL 6700F, Tokyo, Japan), and transmission electron microscopy (TEM, Philips CM300, Amsterdam, Netherlands) were used to characterize the features during each step of fabrication. The TEM was equipped with the DX4 EDS system and Gatan Filter that enabled high-resolution elemental analysis. The SiO_2 control oxide was deposited using a SiO_2 target (99.995% pure) with a copper backing plate in an unbalanced magnetron (UBM) sputtering system (Nanofilm Technologies International Pte. Ltd., Singapore). The variation in film uniformity was typically less than 5%. All depositions were carried out at a chamber base pressure of less than 10^{-6} Torr. X-ray photoelectron spectroscopy (XPS) (AXIS Ultra^{DLD}, Kratos Analytical Ltd., Manchester, UK) measurements were performed using a monochromatized Al Kα X-ray source (1486.71 eV photons) at a constant dwell time of 100 ms and pass energy of 40 eV. The capacitance−voltage and capacitance−time measurements were performed using a precision LCR meter (HP4284A, Hewlett-Packard, USA) under a measurement frequency of 100 kHz.

3. RESULTS AND DISCUSSION

3.1. In Situ Fabrication of ZnO Nanopatterns Using BCP Templates. Well-defined ZnO nanopatterns (Figure 1) with sub-50 nm feature resolutions were realized through selective decomposition of diethyl zinc precursors within PVP core of PS-*b*-PVP reverse micelle arrays on the surface. The schematic of the process steps used for fabrication of ZnO nanopatterns is illustrated in Figure 2.

PS-*b*-PVP reverse micelles were spin coated onto the silicon substrate from *m*-xylene solution with concentration of 0.5% (w/w) at spin speeds of 3000 rpm. The amphiphilic diblock copolymers self-assembled on surfaces upon solvent evaporation. When the process conditions were optimized, the

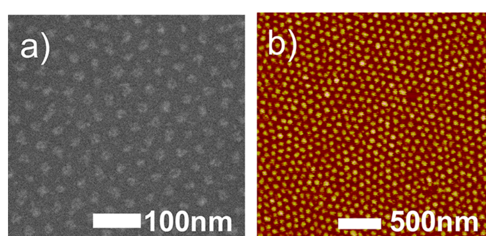

Figure 1. (a) FESEM and (b) AFM images of ZnO nanopatterns obtained through in situ decomposition of Zn precursors into the micelle templates.

coatings exhibited continuous, quasi hexagonally ordered arrays of polymeric features that were used as templates for pattern transfer. The choice of solvent, the concentration of the micelles in the solution, humidity, and the speed of coating can be used as handles to achieve high-resolution changes in the feature size and pitch of the patterns.[41]

The Si chip containing a coating of reverse micelles is exposed to diethyl zinc vapors within an atomic layer deposition (ALD) chamber. The $(C_2H_5)_2Zn$ concentration was controlled by varying the number of cycles of exposure. Each cycle of exposure consisted of one $(C_2H_5)_2Zn$ pulse and one H_2O pulse with a nitrogen purge between each precursor pulse. High degree of control over the vapor concentrations employed in a typical ALD system allowed excellent control over the degree of incorporation of zinc precursor. As a process of optimization, four different experiments along with controls were carried out, wherein the PS-*b*-PVP coatings were subjected to 10, 30, 50, and 100 cycles of exposure. The ALD was performed on bare silicon substrates without templates as controls to determine the growth rate and to confirm that the deposition was indeed highly controlled (refer Figure S2 of the Supporting Information). The $(C_2H_5)_2Zn$ selectively decomposes within the hydrophilic PVP core, thereby anchoring its position defined by the polymer template. The PS thin film being nonselective to zinc precursor acts as a mask preventing any deposition of zinc onto the underlying silicon surface. After incorporation of the zinc precursor, the polymeric template was removed by O_2 plasma etch to obtain ZnO nanoparticle arrays. The micelle templates subjected to 10 cycles did not reveal any patterns while 100 cycles compromised the pattern morphology due to nonselective deposition of ZnO. 50 cycles of ALD on the micelle templates proved to be optimal in revealing well-defined, high density, and discrete nanopatterns of ZnO (refer to Figure S3 of the Supporting Information for details on the optimization of ALD cycles).

The resulting ZnO nanofeatures have a diameter of 38 nm and height of 14 nm for 50 cycle exposure as shown in Figure 3. Characterization by AFM and FESEM (Figure 1a,b) show well-defined nanoarrays uniformly spanning the coated area (refer to Figure S4 of the Supporting Information for an AFM image of the macroscopic array of ZnO). The discrete nature of the ZnO features was further confirmed by performing a cross section TEM with energy dispersive X-ray (EDX) at high spatial resolutions. The EDX spectra acquired on and between the ZnO features showed absence of Zn between features, thereby confirming the pattern integrity as shown in Figure 4.

Since the patterning of ZnO is achieved through polymeric templates, it is essential to check the resulting ZnO nanopatterns for any residual polymeric contamination. XPS analysis of the ZnO nanopatterns showed that no nitrogen was present and confirmed that the oxygen plasma had completely removed the polymer (refer to Figure S5 of the Supporting Information on XPS analysis of ZnO nanopatterns).

The feature size, periodicity, and spacing of ZnO nanopatterns were guided by the polymer templates, and hence, tunability of the geometric attributes in the ZnO arrays is feasible through tailoring the block copolymer self-assembly process. The advantages of this fabrication protocol are derived from the controlled and selective incorporation of the precursor into the micelle core without disturbing the morphology of the polymer template. Since ALD is employed to create patterns, ZnO nanofeatures are mechanically robust. In addition, the nanofeatures are produced on a macroscopic scale in a highly controlled manner offering a high feature resolution that is otherwise difficult to attain through other techniques. Apart from this, the ability to pattern at low operating temperatures

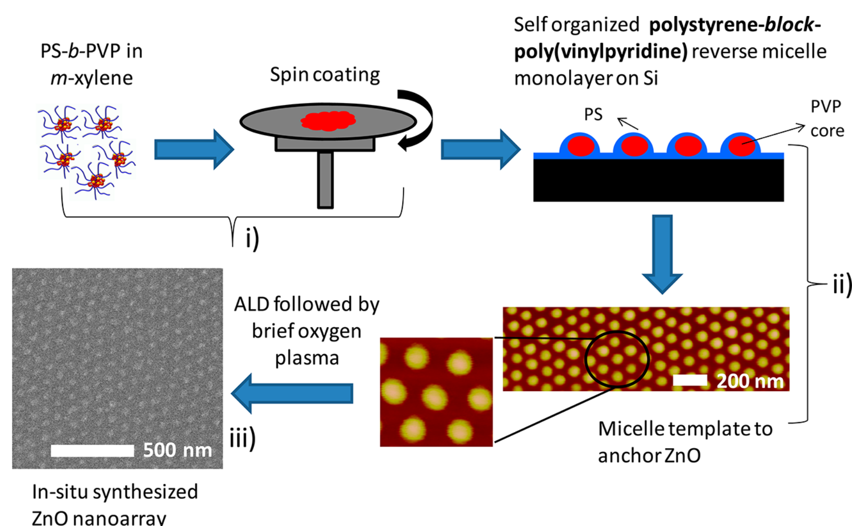

Figure 2. Schematic of the process steps to create ZnO nanopatterns starting with (i) spin coating of PS-*b*-PVP reverse micelles from solution phase to obtain (ii) two dimensionally ordered arrays of chemical templates that yield (iii) ZnO nanoparticle arrays upon decomposition of diethyl Zinc precursors within the micelle core, followed by template removal by oxygen plasma exposure.

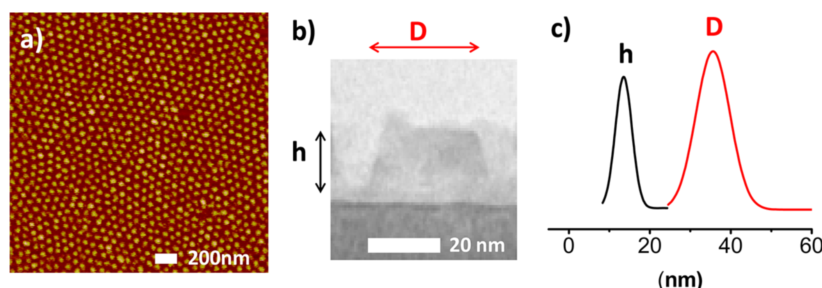

Figure 3. Tapping mode AFM image of ZnO nanopatterns obtained upon 50 cycles of ALD, (b) TEM cross-section of a representative ZnO feature (c) feature size distributions determined by AFM revealing mean values of 38 nm for diameter (‘*D*’) of 14 nm for height (‘*h*’).

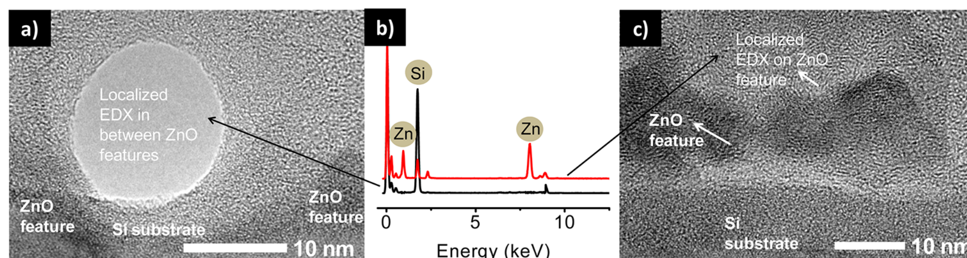

Figure 4. TEM images showing areas where localized EDX analysis was performed (a) in between the ZnO features and (c) on the features. (b) EDX spectra show the absence of Zn in between the features confirming the discreteness of the nanopatterns.

(less than the glass transition temperature of the polymer which is ∼100 °C) positions this protocol ahead of other techniques for patterning on thermally sensitive media such as flexible plastic substrates.

3.2. Metal-Oxide-Semiconductor Capacitor Device Fabrication. The electrical characteristics of the ZnO nanopatterns on p-Si and n-Si substrate were investigated by sandwiching them within a metal-oxide-semiconductor (MOS) test capacitor as illustrated in Figure 5. The capacitance−voltage measurements were performed at 100 kHz for the test capacitors built on p-Si by sweeping the gate voltage from +5 to −10 V and vice versa (Figure 6a). The capacitors incorporating ZnO arrays showed hysteresis of 2.20 V in comparison to a low hysteresis of ∼0.5 V for the control substrates with no ZnO (refer to Figure S6 of the Supporting Information for the control *C*−*V* plot). The counter-clockwise hysteresis observed confirms hole-storage behavior. The small hysteresis observed on the control substrates represent the residual charges in the trap states present in the oxide or at the interface. Similarly, capacitance−voltage measurements were performed on n-Si by sweeping the applied gate voltage between −3 and +3 V. As could be observed from Figure 6b, there is no appreciable hysteresis or flatband voltage (V_{FB}) shift. There is no net charge trapping taking place in the ZnO floating gate. This suggests that no charge injection into the ZnO nanopatterns takes place, and hence, charges are not trapped. The intrinsic n-type nature of the ZnO nanopatterns owing to the presence of zinc interstitials and oxygen vacancies[17] may prevent the negatively charged electrons from being injected from n-Si and be stored in the ZnO traps during the voltage sweep. Moreover, any charges stored in the interface traps or in border traps are rapidly discharged during erasure so that a negligible flat band

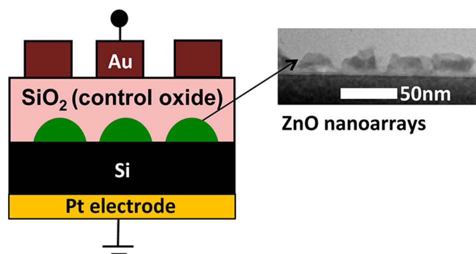

Figure 5. Schematic illustration of capacitor test device incorporating ZnO nanoarrays as charge storage centers. TEM side view of ZnO nanoarrays is shown for reference.

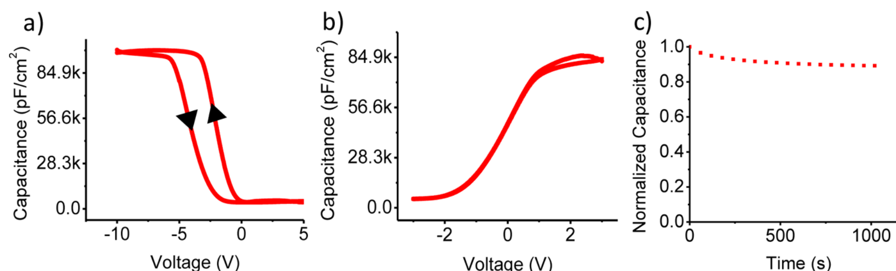

Figure 6. Capacitance−voltage characteristics of the MOS capacitors consisting of ZnO nanoarrays built on (a) p-Si and (b) n-Si substrates. (c) Capacitance−time measurement on MOS capacitor device incorporating ZnO nanoarrays on p-Si substrate with thermally grown tunneling oxide of 3nm thickness

voltage shift is observed.[31] The hysteresis behavior on n-Si is similar to earlier reports on the ZnO capacitor structures.[31,42] The charge storage density was estimated from the area of the hysteresis curve of the capacitor device incorporating ZnO built on p-Si and after normalizing with the volume of the features and was found to be 3.47×10^{18} cm^{-3}. On the basis of the feature density of ZnO as known from the AFM (of ∼2.4×10^{10} cm^{-2}), the charge density translated into an estimated ∼55 holes stored per feature (refer to the Supporting Information for the calculations on charge storage density). This is indicative of high density of trap states that enables high charge storage capacity and demonstrates the potential of the ZnO nanopatterned arrays to act as charge storage centers in flash memory devices.

Capacitance−time measurements for the test structure were performed to study the rate of discharge as a function of time at an applied voltage corresponding to V_{FB} (−2.35 V). The $C-t$ measurements show good retention of ∼90% of the charge at the end of 1000 s (Figure 6c). As an estimate of charge retention as a function of time for longer durations,[43,44] extrapolation of the $C-t$ curve shows retention of 81% at the end of 10 000 s (refer to Figure S6 of the Supporting Information for the extrapolated $C-t$ characteristics). The initial rapid decay of the capacitance indicated that the depletion of charges occurs primarily from shallow trap states. However, charge carriers trapped at deeper levels tend to be more resistant to leakage, and hence, an extrapolated $C-t$ decay represents a worst case scenario when the real $C-t$ behavior is expected to show better retention.[37] Moreover, good charge retention characteristics can also be attributed to the well patterned and spatially isolated nanoarrays when the chances of lateral conduction and charge leakage is almost negligible; at the same time, the device exhibits resilience to stress induced leakage current (SILC).[45,46] The retention characteristics are comparable to the charge trap flash (CTF) memory devices reported in the literature that employ the conventional silicon-oxide-nitride-oxide-silicon (SONOS)[47] or other high-k dielectric[43] as the charge trapping layer.[46] Since the fabrication of ZnO nanoarrays were carried out at low temperatures, the protocol can be extended to flexible plastic substrates. Moreover, incorporation of precursors into the reverse micelles is nonspecific to Zn, and hence, a variety of metal and metal oxide nanoarrays of different materials with specific interest toward charge trapping can be patterned.

4. CONCLUSIONS

The work presents a simple yet highly controlled route to produce high-density nanopatterns of ZnO with excellent pattern definition (low standard deviations in geometric attributes of the features) by incorporating the ALD precursor selectively into the micelle templates. The advantage is derived from the use of ALD that provides a high degree of control and from the use of block copolymer templates which offers tunability of the template that guides and controls the geometric attributes of the resulting ZnO nanopatterns. The precursor dosage, exposure cycles, process parameters, and processing conditions can be manipulated to obtain reproducible patterns of high quality and resolution. Preliminary results of the electrical characteristics of the arrays show their promise as charge storage centers with high storage density and excellent retention characteristics demonstrating significant potential for charge trap flash memories. Further, the capability of the approach to deliver nanopatterns down to sub-50nm resolutions, with flexibility in the choice of materials and substrates, allows catering to functional components within nanoscale devices for other applications such as photovoltaics, catalysis, LEDs, and sensors.

■ ASSOCIATED CONTENT

Supporting Information

Further information about process optimization, characterization, and control experiments pertaining to the study. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: chesmp@nus.edu.sg (M.P.S.); krishnam@lippmann.lu (S.K.).

Notes

The authors declare no competing financial interest.

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